M.A.P

Claims 1-30 are Canceled

31. A semiconductor storage device in which a plurality of word lines are activated together by causing each of the word lines which is once activated to hold the activated state during a plurality of successive word line selection cycles, comprising:

a latch circuit which is configured to derive the logical AND of a signal activated when a corresponding memory block is accessed and a redundancy miss is first made and a signal generated in each cycle to determine timing for activating a sense amplifier in each cycle, and generates and holds a sense amplifier activation signal.

32. The semiconductor storage device according to claim 31, wherein a plurality of word lines in the memory block are activated together.

33. A semiconductor storage device which has function of activating together a plurality of word lines connected to the same bit line pair via cell transistors, comprising:

a column redundancy system which sets repair regions of column redundancy based on row addresses,

wherein the repair regions are set to permit the plurality of word lines activated together to belong to the same repair region when the repair regions are set to divide the bit line.

34. The semiconductor storage device according to claim 33, wherein the repair regions are set to cause the number of partial repair regions linked to configure one repair region to be suppressed to minimum.

35. The semiconductor storage device according to claim 33, wherein the repair regions are set to cause word lines which can be activated together in the memory cell array and used for reading/writing independent data simultaneously to belong to the same repair region.

Claims 36-49 are Canceled